Remarks

Claims 1, 4, 6, 9, 11 and 16 are amended herein. Claims 1-2, 4-12, 14-17 and 19-20 remain pending in the Application. No new matter has been added as a result of the Claim amendments.

Rejection under 103(a)

Claims 1-2, 4-12, 14-17 and 19-20

In the Office Action, the Examiner rejected Claims 1-2, 4-12, 14-17 and 19-20 under 35 USC 103(a) as being unpatentable over Wu (hereinafter Tremblay) (6668372) in view of Holmberg et al (hereinafter Holmberg) (2001/0021959) and further in view of Burke et al (hereinafter Burke) (6738865). Applicants have reviewed the cited reference and respectfully submit that the present invention is not rendered obvious over Wu in view of Holmberg and further in view of Burke for the following rationale.

Applicants respectfully state that currently amended Claim 1 (Claims 6, 11 and 16 include similar features) includes the features of "method to analyze a computer program that includes a plurality of blocks of code, the method comprising:

receiving a block of code to a code cache;

using a counter for tracking each time said block of code is executed on said code cache, wherein said counter is not required to be added to said block of code in said code cache;

maintaining a counter cache for storing each said counter of said block of code while said block of code is stored on said code cache, wherein said counter cache is distinct from said code cache; and

maintaining a storage area for storing each said counter of said block of code previously executed on said code cache after said block of code is evicted from said code cache, wherein said storage area is distinct from said code cache and said counter cache." Support for the Claimed features is found throughout

the Specification and Figures including Figure 3 and page 10 line 17 through page 11 line 25 of the Specification.

Applicants understand the Examiner to state in the office action that Wu does not explicitly disclose that the code memory is a code cache, nor does Wu disclose that the counter is maintained in a cache.

However, Applicants disagree with the Examiner's statement that Holmberg overcomes the shortcomings of Wu. Applicants understand the Examiner to state on page 8 lines 15-20 of the office action mailed 6/17/2004 that Holmberg does not disclose maintaining a counter cache for storing a counter associated with a block of code, nor does Holmberg disclose maintaining a storage area for storing counters associated with a block of code.

For this reason, Applicants respectfully submit that Wu in view of Holmberg does not teach or render obvious the claimed features of Claims 1, 6, 11 and 16. As such, Applicants respectfully submit that Claims 1, 6, 11 and 16 overcome the rejection under 35 U.S.C. §103(a) and are therefore allowable.

Additionally, Applicants have further reviewed Wu and understand Wu to teach, as shown in Figures 4A-4D, that a profile portion (e.g., 407) is added to the branch instruction. Applicants respectfully submit that the addition of a profile portion to the branch instruction teaches directly away from the claimed feature of using a counter for tracking each time said block of code is executed on said code cache, wherein said counter is not required to be added to said block of code in said code cache and maintaining a counter cache for storing each said counter of said block of code while said block of code is stored on said code cache, wherein said counter cache is distinct from said code cache.

A plurality of reasons for the claimed features including increased data locality and reduced developer and recompile time are found in the Specification.

For this reason, Applicants submit that the teachings of Wu do not render obvious three distinct storage locations and a counter that is not required to be added to the block of code.

As previously stated, Applicants disagree with the Examiner's statement that Holmberg overcomes the shortcomings of Wu. Applicants understand the Examiner to state on page 8 lines 15-20 of the office action mailed 6/17/2004 that Holmberg does not disclose maintaining a counter cache for storing a counter associated with a block of code, nor does Holmberg disclose maintaining a storage area for storing counters associated with a block of code.

Furthermore, Burton does not overcome the shortcomings of Wu and Holmberg. Specifically, the Examiner has not relied on, and the Applicants do not understand Burton to teach or render obvious a plurality of storage locations and a counter that is not required to be added to the block of code.

For this additional reason, Applicants respectfully submit that Wu in view of Holmberg does not teach or render obvious the claimed features of Claims 1, 6, 11 and 16. As such, Applicants respectfully submit that Claims 1, 6, 11 and 16 overcome the rejection under 35 U.S.C. §103(a) and are therefore allowable.

Regarding Claims 4, 9, 14 and 19, Applicants respectfully submit that Claims 4, 9, 14 and 19 include the feature "determining which said counter of said block of code stored on said counter cache is least recently executed; evicting said least recently executed block of code, related to said counter, from said code cache; and copying said counter of said least recently executed block of code from said counter cache to said storage area when said least recently executed block of code related to said counter is evicted from said code cache."

Applicants respectfully assert that there is no motivation to combine the teachings of Wu, Holmberg and Burke to teach or render obvious the present

claimed features of Claims 4, 9, 14 and 19. Applicants understand Holmberg to teach against the use of caching data based solely on frequency of use. That is, Applicants understand Holmberg to also teach cache allocation based on importance of the instruction such as, for example, the processor can do measurements that do not count accesses from these program blocks or discard accesses made from programs running on lower priority levels. Therefore, Holmberg does not teach nor render obvious the features of the present invention. In fact, Holmberg teaches away from the claimed feature of evicting least recently executed blocks of code.

Thus, Applicants respectfully assert that nowhere does the combination of Wu and Holmberg and Burton teach, disclose or suggest the present invention as recited in independent Claims 4, 9, 14 and 19, and that these claims overcome the rejection under 35 U.S.C. § 103(a), and are thus in condition for allowance.

Applicants respectfully point out that Claims 2 and 4-5 depend from the allowable Independent Claim 1, Claims 7-10 depend from the Independent Claim 6, Claims 12 and 14-15 depend from the allowable Independent Claim 11 and Claims 16-17 and 19-20 depend from the allowable Independent Claim 16 and recite further features of the present claimed invention. Therefore, Applicants respectfully state that Claims 2, 4-12, 14-17 and 19-20 are allowable as pending from allowable base Claims.

Conclusion

In light of the above amendments and remarks, Applicants respectfully request allowance of Claims 1-2, 4-12, 14-17 and 19-20.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Respectfully submitted,
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